Application Serial No. 10/813,291

IN THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the above-referenced application:

1. (Currently amended) A loop filter for use in a phase-locked loop circuit, the loop filter comprising:

a resistive element;

at least one metal-oxide-semiconductor (MOS) transistor configured as a capacitor having a first capacitance associated therewith, the at least one MOS transistor being connected between a voltage source and an input of the loop filter via the resistive element; and

a bias circuit connected to the at least one MOS transistor, the bias circuit being configured for maintaining a substantially constant reference voltage across the MOS transistor, the reference voltage ~~being selected so as to bias~~ biasing the at least one MOS transistor in a designated region of operation ~~for optimizing the first~~ wherein a capacitance per unit area of the at least one MOS transistor is optimized.

2. (Original) The loop filter of claim 1, wherein the at least one MOS transistor comprises a thick-oxide MOS device, and wherein the reference voltage is selected to substantially maximize the first capacitance per unit area.

3. (Currently amended) The loop filter of claim 1, wherein the at least one MOS transistor comprises a thick-oxide NMOS device, and wherein the reference voltage is greater than or about equal to a magnitude of a difference between a threshold voltage of the MOS transistor and the ~~substantially constant~~ voltage source.

4. (Currently amended) The loop filter of claim 1, wherein the at least one MOS transistor comprises a thick-oxide PMOS device, and wherein the reference voltage is less than or about equal to a magnitude of a difference between a threshold voltage of the MOS transistor and the ~~substantially constant~~ voltage source.

5. (Original) The loop filter of claim 1, wherein the designated region of operation for biasing the at least one MOS transistor comprises a high-capacitance region in which the first capacitance is substantially maximized per unit area.

6. (Currently amended) The loop filter of claim 1, wherein the at least one MOS transistor comprises a thin-oxide MOS device, the bias circuit being configured for maintaining ~~a~~ <u>the</u> substantially constant reference voltage across the at least one MOS transistor, the reference voltage being selected so as to substantially minimize a tunneling leakage current in the at least one MOS transistor.

7. (Original) The loop filter of claim 1, wherein the voltage source is ground.

8. (Original) The loop filter of claim 1, wherein the bias circuit comprises an amplifier including a first input for receiving a voltage across the at least one MOS transistor, a second input for receiving the reference voltage, and an output for generating a signal proportional to a difference between the respective voltages at the first and second inputs of the amplifier.

9. (Original) The loop filter of claim 8, wherein the amplifier comprises a transconductance amplifier, the loop filter further comprising a second capacitance including a first terminal coupled to the output of the amplifier and a second terminal coupled to the voltage source.

10. (Original) The loop filter of claim 1, further comprising a second MOS transistor configured as a capacitor having a second capacitance associated therewith, the second MOS transistor being connected between the input of the loop filter and the voltage source and in parallel with the first MOS transistor.

11. (Original) The loop filter of claim 10, wherein the second capacitance is substantially less than the first capacitance.

12. (Original) The loop filter of claim 10, wherein the second capacitance is about 100 times less than the first capacitance.

13. (Original) The loop filter of claim 1, wherein the voltage source is one of a positive supply voltage and a negative supply voltage of the loop filter.

14. (Original) The loop filter of claim 1, wherein the resistive element comprises at least one resistor.

15. (Original) The loop filter of claim 1, wherein the resistive element comprises at least one MOS transistor biased in a substantially linear region of operation.

16. (Currently amended) A phase-locked loop circuit, comprising:

a variable frequency generator including a first input for receiving a first control signal presented thereto, a second input for receiving a second control input presented thereto, and an output for generating an output signal having a frequency associated therewith which varies as a function of the first and second control signals;

a phase-frequency detector including a first input for receiving a reference signal having a reference frequency associated therewith, a second input for receiving at least a portion of the output signal from the variable frequency ~~oscillator~~ generator, and an output for generating the first control signal, the first control signal being representative of a difference between the reference frequency and the frequency of the output signal; and

a loop filter including an input for receiving the first control signal and an output for generating the second control signal, the loop filter comprising:

a resistive element;

at least one metal-oxide-semiconductor (MOS) transistor configured as a capacitor having a first capacitance associated therewith, the at least one MOS transistor being connected between a voltage source and an input of the loop filter via the resistive element; and

a bias circuit connected to the at least one MOS transistor, the bias circuit being configured for maintaining a substantially constant reference voltage across the MOS transistor, the reference voltage ~~being selected so as to bias~~ biasing the at least one MOS transistor in a designated region of operation ~~for optimizing the first~~ wherein a capacitance per unit area of the at least one MOS transistor is optimized.

17. (Original) The circuit of claim 16, wherein the at least one MOS transistor in the loop filter comprises a thick-oxide MOS device, and wherein the reference voltage is selected to substantially maximize the first capacitance per unit area.

18. (Original) The circuit of claim 16, wherein the designated region of operation for biasing the at least one MOS transistor in the loop filter comprises a high-capacitance region in which the first capacitance is substantially maximized per unit area.

19. (Original) The circuit of claim 16, wherein the bias circuit in the loop filter comprises an amplifier including a first input for receiving a voltage across the at least one MOS transistor, a second input for receiving the reference voltage, and an output for generating a signal proportional to a difference between the respective voltages at the first and second inputs of the amplifier.

20. (Currently amended) An integrated circuit including at least one loop filter, the at least one loop filter comprising:

a resistive element;

at least one metal-oxide-semiconductor (MOS) transistor configured as a capacitor having a first capacitance associated therewith, the at least one MOS transistor being connected between a voltage source and an input of the loop filter via the resistive element; and

a bias circuit connected to the at least one MOS transistor, the bias circuit being configured for maintaining a substantially constant reference voltage across the MOS transistor, the reference voltage ~~being selected so as to bias~~ biasing the at least one MOS transistor in a designated

region of operation ~~for optimizing the first~~ <u>wherein a</u> capacitance per unit area <u>of the at least one MOS transistor is optimized</u>.

21. (Original) The integrated circuit of claim 20, wherein the at least one MOS transistor in the at least one loop filter comprises a thick-oxide MOS device, and wherein the reference voltage is selected to substantially maximize the first capacitance per unit area.

22. (Original) The integrated circuit of claim 20, wherein the designated region of operation for biasing the at least one MOS transistor in the at least one loop filter comprises a high-capacitance region in which the first capacitance is substantially maximized per unit area.

23. (Currently amended) An integrated circuit including at least one phase-locked loop, the at least one phase-locked loop comprising:

a variable frequency generator including a first input for receiving a first control signal presented thereto, a second input for receiving a second control input presented thereto, and an output for generating an output signal having a frequency associated therewith which varies as a function of the first and second control signals;

a phase-frequency detector including a first input for receiving a reference signal having a reference frequency associated therewith, a second input for receiving at least a portion of the output signal from the variable frequency ~~oscillator~~ <u>generator</u>, and an output for generating the first control signal, the first control signal being representative of a difference between the reference frequency and the frequency of the output signal; and

a loop filter including an input for receiving the first control signal and an output for generating the second control signal, the loop filter comprising:

a resistive element;

at least one metal-oxide-semiconductor (MOS) transistor configured as a capacitor having a first capacitance associated therewith, the at least one MOS transistor being connected between a voltage source and an input of the loop filter via the resistive element; and

a bias circuit connected to the at least one MOS transistor, the bias circuit being configured for maintaining a substantially constant reference voltage across the MOS transistor, the reference voltage ~~being selected so as to bias~~ <u>biasing</u> the at least one MOS transistor in a designated region of operation ~~for optimizing the first~~ <u>wherein a</u> capacitance per unit area <u>of the at least one MOS transistor is optimized</u>.